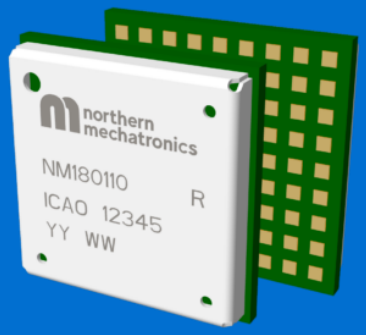
DATASHEET

NM180110

LoRa® Bluetooth® 5 Low Energy Module



Overview

LoRa®

- **Transceiver**: Semtech SX1262 Long Range Low Power LoRa® Transceiver +22dBm, global frequency coverage
- **Frequency**:
  - North America: 902 – 928 MHz
  - Europe: 863 – 870 MHz
- **Maximum Transmit Power**: 21.7 dBm
- **Receiver Sensitivity**: -147.6 dBm

Bluetooth®

- **Specification**: Bluetooth® 5 Low Energy
- **Frequency**: 2.402 – 2.480 GHz
- **Maximum Transmit Power**: 3 dBm
- **Receiver Sensitivity**: -95 dBm

Power

- **Supply Voltage**: 1.8 – 3.6V
- **Current Consumption**:
  - Processor: 6uA / MHz
  - Sleep: 5uA (Typical)
  - BLE: 7 – 9 mA (Transmit)
  - LoRa: 41 – 143 mA (Transmit)

Processor

- **Architecture**: Ambiq Apollo3 Blue Plus ARM® Cortex® M4 (FPU, max 96MHz)
- **Memory**: Flash: 2 MB, RAM: 768 kB
- **Security**: ISO 7816 secure interface, secure key storage, secure boot, secure OTA, external flash inline encryption
- **Interfaces**: 42x GPIO, 2x UART with flow control, 4x I2C master, 3x SPI master, 1x Dual/Quad/Octal SPI master, 1x SPI/I2C slave, 1x PDM master, 1x I2S slave
- **Peripherals**: 10-channel 14-bit ADC, voltage comparator, temperature sensor

Environmental

- **Operating Temperature**: -40°– 85°C

Physical

- **Dimensions**:
  12.8 mm x 12.8 mm x 2.4 mm (LGA 81)

1 Features

Category	Parameter	Value
LoRa®	Transceiver	Semtech SX1262 Long Range Low Power LoRa® Transceiver +22dBm, global frequency coverage
	Frequency	North America: 902–928 MHz, Europe: 863–870 MHz
	Max Transmit Power	21.7 dBm
	Receiver Sensitivity	-147.6 dBm (BW=10.4kHz, SF=12)
Bluetooth® Low Energy	Specification	Bluetooth® 5 Low Energy
	Frequency	2.402 – 2.480 GHz
	Max Transmit Power	3 dBm
	Receiver Sensitivity	-95 dBm
Host Processor	Architecture	Ambiq Apollo3 Blue Plus ARM® Cortex® M4 with FPU Up to 96MHz
	Memory	Flash: 2 MB on-chip with external flash support RAM: 768 kB
	Interfaces	42x GPIO 1x Dual/Quad/Octal SPI master 3x SPI Master 4x I2C Master 1x SPI/I2C Slave 2x UART with flow control 1x PDM Master 1x I2S Slave
	Security	ISO 7816 Secure Interface Secure Key Storage Secure Boot Secure OTA External Flash Inline Encryption/Decryption
	Peripherals	10-Channel 14-bit ADC at 1.2MS/s Voltage Comparator Temperature Sensor
Power	Supply Voltage	1.8 – 3.6V
	Current Consumption	Processor: 6uA / MHz BLE: Tx 0 dBm 7mA, Rx 3 mA LoRa: Tx 22 dBm 143 mA, Rx 125 kHz 8.8 mA Sleep: 5uA (deep sleep mode 2, RAM retention, RF section OFF)
Environmental	Operating Temperature	-40° to 85°C
Physical	Dimensions	12.8 mm x 12.8 mm x 2.4 mm (LGA 81)

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5 Pin Definition

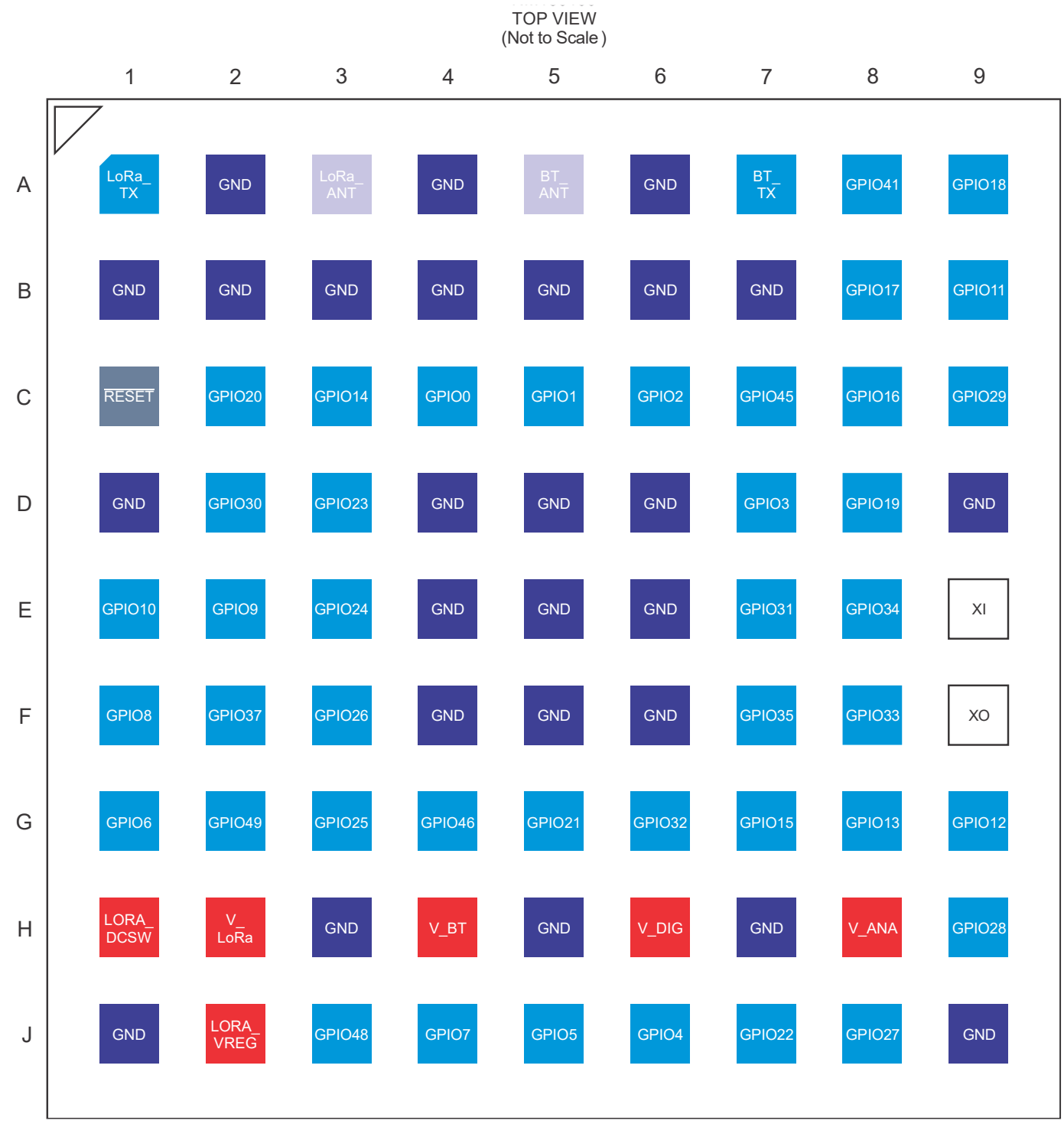

Figure 1: NM180110 Pin Diagram

Table 1: NM180110 Pin Definition

Pin Number	Type	Name	Description
A2, A4, A6, B1, B2, B3, B4, B5, B6, B7, D1, D4, D5, D6, D9, E4, E5, E6, F4, F5, F6, H3, H5, H7, J1, J9	PWR	GND	Ground connections.
H6	PWR	V_DIG	Supply input for the Apollo3 digital section.
H8	PWR	V_ANA	Supply input for the Apollo3 analog section.
H4	PWR	V_BT	Supply input for the Apollo3 Bluetooth section.
H2	PWR	V_LORA	Supply input for the LoRa transceiver.
C1	I	$\overline{\text{RESET}}$	Apollo3 active low chip reset.
E9	I	XI	Crystal.
F9	O	XO	Crystal.
A3	RF	LORA_ANT	LoRa antenna connection.
A1	O	LORA_TX	LoRa transmit indicator.
A5	RF	BT_ANT	Bluetooth antenna connection.
A7	O	BT_TX	Bluetooth transmit indicator.
A8, A9, B8, B9, C2, C3, C4, C5, C6, C7, C8, C9, D2, D3, D7, D8, E1, E2, E3, E7, E8, F1, F2, F3, F7, F8 G1, G2, G3, G4, G5, G6, G7, G8, G9, H9, J3, J4, J5, J6, J7, J8	I/O	GPIO0 – GPIO49	General purpose inputs and outputs.
H1	PWR	LORA_DCSW	SX1262 DC/DC switcher output.
J2	PWR	LORA_VREG	SX1262 regulated output voltage from the internal regulator.

6 Electrical Characteristics

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_DIG	Digital Supply		-	3.63	V
V_ANA	Analog Supply		-	3.63	V
V_BT	Bluetooth Supply		-	3.63	V
V_LORA	LoRa Supply		-	3.9	V
T_S	Storage Temperature		-55	125	°C
T_OP	Operating Temperature		-40	85	°C
ESD_LU	Latch-up	JEDEC standard JESD78 B, Class I Level A	-	100	mA
ESD_HBM	ESD Human Body Model	ANSI/ESDA/JEDEC Standard JS-001-2014 Class 2	-	2.0	kV
ESD_CDM	ESD Charged Device Model	JEDEC Standard JESD22-C101D, Class 3	-	250	V
T_REFLOW	Reflow temperature	Reflow Profile per JEDEC J-STD-020D.1	-	260	°C

Table 3: Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_DIG	Supply input for the digital section		1.8	3.3	3.6	V
V_ANA	Supply input for the analog section		1.8	3.3	3.6	V
V_BT	Supply input for the BLE section		1.8	3.3	3.6	V
V_LORA	Supply input for the LoRa section		1.8	3.3	3.6	V
f_XTAL	Low frequency external crystal		-	32.768	-	kHz
T_A	Ambient operating temperature		-40	-	85	°C

6.1 RF Performance Characteristics

6.1.1 Bluetooth RF Characteristics

Table 4: Bluetooth Transmitter Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BT_P_{OUT}_MAX	Maximum transmit power	CW, matching and RF switch loss included	1.7	2	2.5	dBm
BT_P_{OUT}_MIN	Minimum active transmit power	CW	-11	-	-	dBm
BT_P_{OUT}_STEP	Output power step size	CW	-	1	-	dB
BT_P_{OUT}_VAR_F	Output power variation vs RF frequency at BT_POUT_MAX	CW	-0.5	-	0.5	dB
	Second harmonic	CW	-	-40	-30	dBm
	Third harmonic	CW	-	-40	-30	dBm
BT_F_RANGE	RF tuning frequency range	CW	2400	-	2483.5	MHz

Table 5: Bluetooth Receiver Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BT_SAT	Max usable receiver input level at 0.1% BER		-	0	-	dBm
BT_SENS	30.8% packet error rate		-92	-93	-94	dBm
BT_C/I_CC	Signal to co-channel interferer, 0.1% BER		-	7	-	dB
BT_BLOCK_OOB	Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range.	30 MHz to 2000 MHz	-	-5	-	dBm
		2003 MHz to 2399 MHz	-	-15	-	dBm
		2484 MHz to 2997 MHz	-	-15	-	dBm
		3000 MHz to 12.75 GHz	-	-5	-	dBm
BT_RSSI_MAX	Upper limit of input power range over which RSSI resolution is maintained		-	-	0	dBm
BT_RSSI_MIN	Lower limit of input power range over which RSSI resolution is maintained		-94	-	-	dBm
BT_RSSI_RES	RSSI resolution		-	1	-	dB

6.1.2 LoRa RF Characteristics

Table 6: LoRa Transmitter Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LORA_POUT_MAX	Maximum transmit power	CW, matching and RF switch loss included	21.0	-	21.7	dBm
LORA_POUT_MIN	Minimum active transmit power	CW	-9	-	-	dBm
LORA _POUT_STEP	Output power step size		-	1	-	dB
LORA _POUT_VAR_V	Output power variation vs supply at LORA_POUT_MAX		-	0.5	-	dB
LORA _POUT_VAR_T	Output power variation vs temperature at LORA_POUT_MAX		-	1	-	dB
LORA _POUT_VAR_F	Output power variation vs RF frequency at LORA_POUT_MAX		-0.5	-	0.5	dB
LORA_SPUR_HRM	Second harmonics	CW at 864.1 MHz, 22 dBm	-	-35	-30	dBm
		CW at 868.5 MHz, 22 dBm	-	-35	-30	dBm
		CW at 902.3 MHz, 22 dBm	-	-35	-30	dBm
		CW at 914.9 MHz, 22 dBm	-	-35	-30	dBm
		CW at 927.5 MHz, 22 dBm	-	-35	-30	dBm
	Third harmonics	CW at 864.1 MHz, 22 dBm	-	-35	-30	dBm
		CW at 868.5 MHz, 22 dBm	-	-35	-30	dBm
		CW at 902.3 MHz, 22 dBm	-	-35	-30	dBm
		CW at 914.9 MHz, 22 dBm	-	-35	-30	dBm
		CW at 927.5 MHz, 22 dBm	-	-35	-30	dBm
LORA _F_RANGE	RF tuning frequency range		830	-	930	MHz

Table 7: LoRa Receiver Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LORA_SAT	Max usable receiver input level		-	10	-	dBm
LORA _RSSI_MAX	Upper limit of input power range over which RSSI resolution is maintained		-	-	0	dBm
LORA _RSSI_MIN	Lower limit of input power range over which RSSI resolution is maintained	10.4 kHz bandwidth and spreading factor of 12	-148	-	-	dBm
LORA _RSSI_RES	RSSI resolution		-	0.5	-	dB

6.2 Current Consumption

Table 8: LoRa Radio Current Consumption at 3.3V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LORA_I_TX	Current consumption in transmit mode, continuous carrier wave at 914.9 MHz	0 dBm	-	41	-	mA
		5 dBm	-	55	-	mA
		10 dBm	-	73	-	mA
		15 dBm	-	98	-	mA
		22 dBm	-	143	-	mA

Table 9: BLE Radio Current Consumption at 3.3V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BLE_I_TX	Current consumption in transmit mode, continuous carrier wave at 2.44 GHz	0 dBm programmed	-	7	-	mA
		3 dBm programmed	-	8	-	mA
		4 dBm programmed	-	9	-	mA

7 Functional Description

7.1 Introduction

The NM180110 module is a highly integrated system-in-package, combining an Ambiq Apollo3 Blue Plus processor with expanded memory and built-in Bluetooth Low Energy (BLE), and a Semtech SX1262 LoRa transceiver, supporting the 868MHz and 915MHz ISM bands. The Apollo3 Blue Plus possesses a secure interface (ISO 7816) including secure boot and secure OTA firmware upgrade over BLE [1]. Large on-chip memory and full programmability allows the NM180110 module to function as application processor, while maintaining all RF, mixed-signals, and digital functions in a single device.

The operating system, radio drivers and wireless communication protocol stacks are provided in Northern Mechatronics SDK and reference application source code. This enables the system integrator to fully leverage the module's existing regulatory grants (e.g. FCC, IC) where applicable.

7.2 Block Diagram

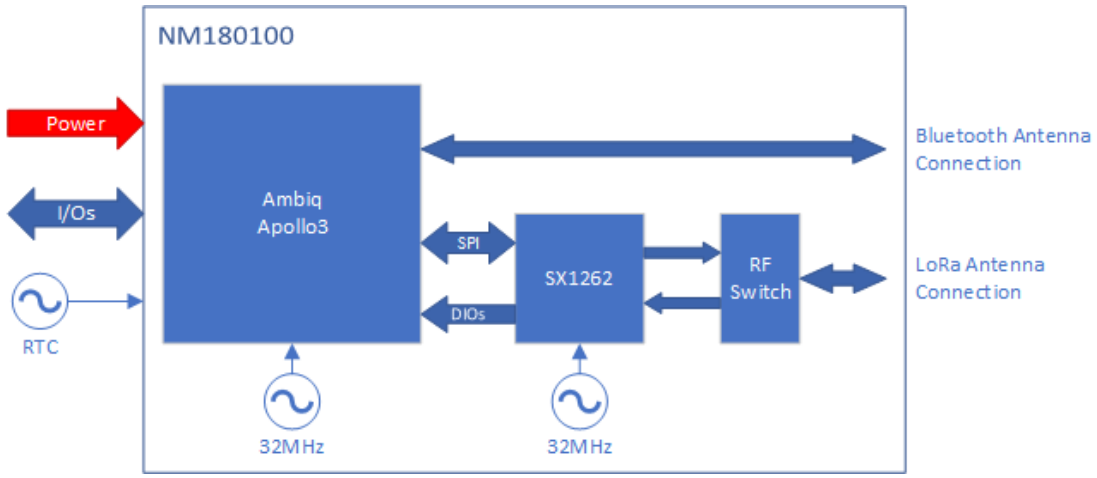

Figure 2: NM1801x0 Block Diagram

7.3 LoRa® Radio

The NM180110 utilizes the Semtech SX1262 transceiver for LoRa communications, which supports the 868MHz and 915MHz ISM bands and has a maximum transmit power of 22dBm [2]. A 32MHz crystal is integrated as the frequency reference for the SX1262 radio and serves as the main clock source for the baseband controller. The SX1262 interfaces with the Apollo3 Blue Plus as an SPI slave, communicating through IOM3 in SPI mode, and SX1262 pins DIO1 and DIO3 are connected to the Apollo3 Blue Plus as interruptible GPIO lines.

Table 10: LoRa Transceiver Interface Pin Assignments

Pin Assignment	SX1262 Pin Name	Description
GPIO36	NSS	SPI slave select.
GPIO38	MOSI	SPI slave input.
GPIO43	MISO	SPI slave output.
GPIO42	SCK	SPI clock input.
GPIO39	BUSY	Radio busy indicator.
GPIO40	DIO1	Multipurpose digital I/O.
GPIO47	DIO3	Multipurpose digital I/O.
GPIO44	NRESET	Radio reset signal, active low.

The NM180110 module contains an integrated LoRa RF front end, consisting of a transmit and a receive path. Transmit and receive selection is controlled by the SX1262 transceiver using DIO2, connected to the on-chip RF switch. The SX1262 LoRa transmit signal is exposed externally to the module to facilitate system integration of multi-radio applications where transmit co-existence is a requirement.

A lattice-type balun circuit is connected between the RF switch and the SX1262 receiver. The circuit provides transformation from a single-ended mode signal into a differential mode that is required by the SX1262 receiver. The balun circuit also provides optimal noise figure matching of the LNA input to maximize the receiver sensitivity performance.

An impedance transforming filter is connected to the SX1262 transmitter output. The filter is conjugately matched to the maximum output power impedance of the power amplifier. It provides optimal power transfer to the antenna and reduces higher harmonics to meet regulatory emission requirements.

7.4 Bluetooth® Low Energy Radio

The NM180110 module includes a Bluetooth Low Energy (BLE) radio that is integrated into the Apollo3 Blue Plus processor. The BLE controller supports up to eight simultaneous connections. The BLE presents to the host as a Host Controller Interface. It also supports extended PDU length and enhanced security.

7.5 Real-Time Clock Input

The NM180110 provides an optional low frequency real-time clock connection for the Apollo3 Blue Plus processor. The RTC clock source must be an external 32.768kHz crystal having a maximum loading capacitance of 7pF.

7.6 Power Supply Sequence

The NM180110 module has four separate supply rails. The baseband digital supply, V_DIG, and analog supply, V_ANA, should be powered up simultaneously. The optimal sequence has V_DIG and V_ANA powered up first. The Bluetooth supply, V_BT, can be powered up simultaneously with V_DIG and V_ANA, or later. The LoRa supply, V_LORA, is typically powered up last.

No device damage occurs if the above sequence is not followed. However, failure to follow this sequence may result in higher power-up currents.

There is no required power-down sequence. However, it is recommended to shut down V_LORA first to avoid undefined digital control line output states.

V_BT and V_LORA sections can each be independently shut down when the corresponding radio is not used, without impacting any other functionalities. It is recommended to shut down V_LORA during long periods of inactivity is to reduce power consumption from the internal RF switch.

7.7 Debugging, Real-Time Tracing, and System Analysis

7.7.1 Serial Wire Debug

Serial Wire Debug (SWD) port consists of a clock and a bi-directional data pin that offers target debugging and low bandwidth trace connectivity. SWD uses an ARM standard bi-directional wire protocol [3] to pass data to and from the debugger and the target system. While the SWD provides real-time access to the system memory without halting the processor, it does not provide real-time tracing.

7.7.2 Serial Wire Output

The Serial Wire Output (SWO) is a trace data drain with no formatter and no pattern generator. It is meant to be used as a part of the Serial Wire Viewer to enable real-time tracing.

7.7.3 Instrumentation Trace Macrocell

The Instrumentation Trace Macrocell (ITM) is a software application driven trace source. This block can be used to provide:

- Printf style debugging
- OS and application events tracing
- System diagnostic information

7.7.4 Serial Wire Viewer

Serial Wire Viewer (SWV) is a real-time tracing technology that uses the SWD port and the SWO pin. SWV provides advanced system analysis and real-time tracing without the need to halt the processor to extract certain types of debug information. With debuggers supporting SWV, the following types of information can be retrieved:

- Periodic samples of the program counter value
- Event notification on memory access (such as reading or writing of a variable)
- Event notification on exception entry and exit
- Event counters
- Timestamp and CPU cycle information

7.7.5 Debug Port Pin Configuration

On power up, the clock (SWDCK) and data signals (SWDIO) of the SWD port must be connected to GPIO20 and GPIO21 respectively. Alternatively, GPIO14 and GPIO15 can be used for SWDCK or SWDIO respectively. However, these pins are not selected by default.

Table 11: Debug Port Pin Configuration Options

Function	Pin Number	Pin Name	Register Field	Value
SWDCK (Default)	C2	GPIO20	PAD20FNCSEL	0
			PAD20INPEN	1
			PAD20PULL	1
SWDIO (Default)	G5	GPIO21	PAD21FNCSEL	0
			PAD21INPEN	1
			PAD21PULL	1
SWDCK (Alternative)	C3	GPIO14	PAD14FNCSEL	6
			PAD14INPEN	1
			PAD14PULL	1
SWDIO (Alternative)	G7	GPIO15	PAD15FNCSEL	6
			PAD15INPEN	1
			PAD15PULL	1

The optional SWO pin can be re-configured dynamically at runtime after the Apollo3 Blue Plus is booted into the application code. The default SWO pin assigned by the boot loader is GPIO46.

Table 12: SWO Pin Configuration Options

Pin Number	Pin Name	Register Field	Value
G7	GPIO15	PAD15FNCSEL	7
J7	GPIO22	PAD22FNCSEL	7
E3	GPIO24	PAD24FNCSEL	7
F8	GPIO33	PAD33FNCSEL	7
A8	GPIO41	PAD41FNCSEL	7
C7	GPIO45	PAD45FNCSEL	7
G4	GPIO46	PAD46FNCSEL	7

8 Package Information

8.1 Mechanical Specifications

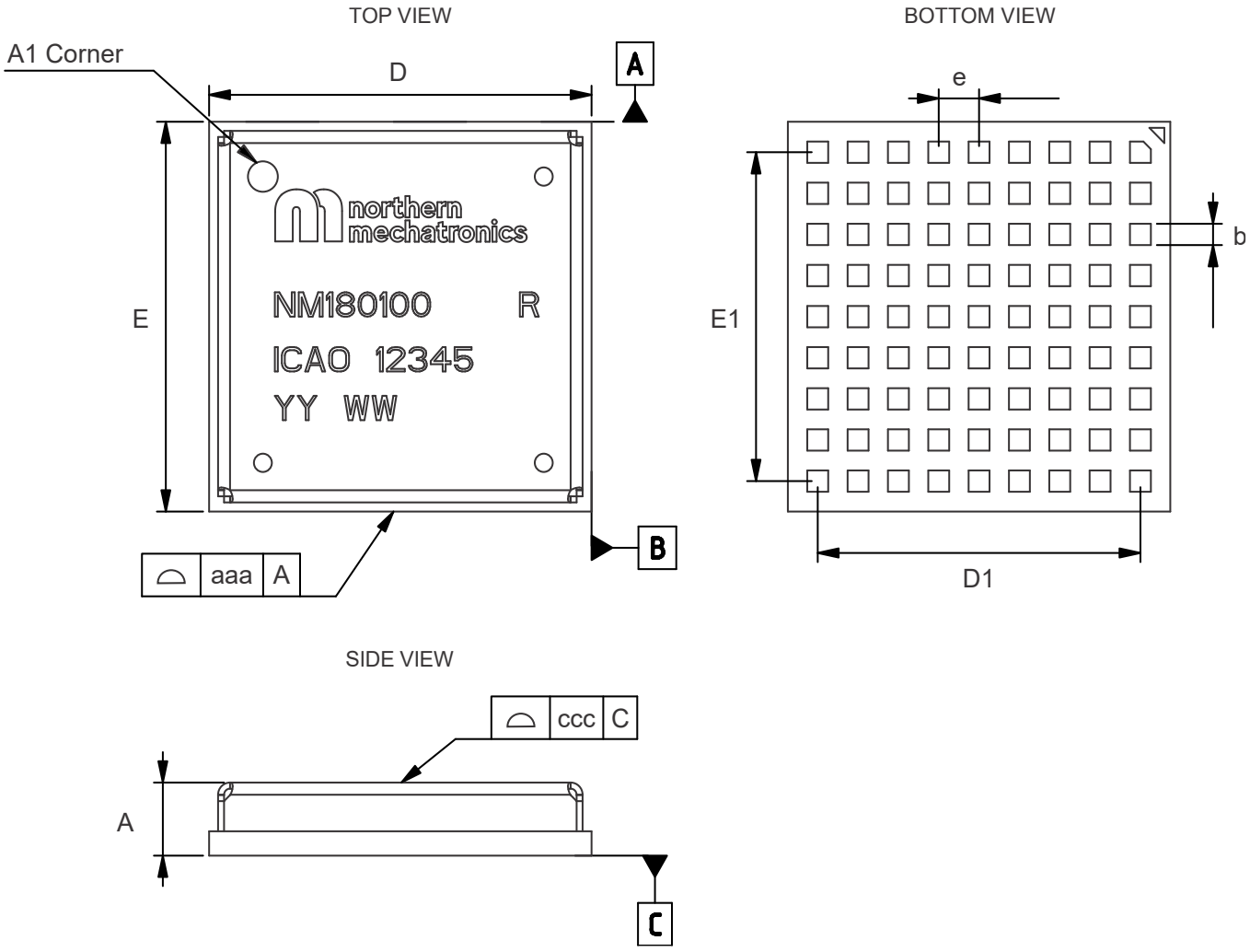

Figure 3: NM1801xx Package Mechanical Specifications (LGA 81, 12.8mm x 12.8mm)

Table 13: Package Mechanical Data

Dimension (mm)	A	b	D	D1	E	E1	e	aaa	ccc
Typ	2.4	0.7	12.8	10.8	12.8	10.8	1.35	0.08	0.08
Min	2.3	-	12.6	10.7	12.6	10.7	-	-	-
Max	2.5	-	13.0	10.9	13.0	10.9	-	-	-

8.2 Land Pattern Recommendations

A non-solder mask defined (NSMD) land pattern is recommended. NSMD pads have a solder mask opening that is larger than the pad and thereby allowing a tighter control of the copper artwork registration compared to the positional tolerance of the solder masking process. NSMD pad definition introduces less stress concentration points in solder joints that may otherwise crack under extreme fatigue conditions.

NSMD pads require a clearance between the copper pad and the solder mask to avoid overlapping between the solder joint and the solder mask. The clearance amount (typically 3 mils) is dependent on the solder mask registration tolerances and may vary from one PCB vendor to another.

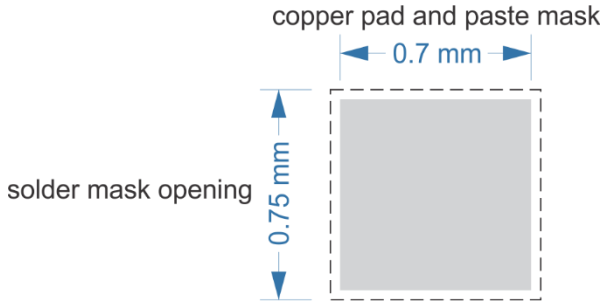

Figure 4: NSMD Land Pattern Recommendation

8.3 Device Marking

Figure of top side device marking with respect to the A1 position identifier shown below.

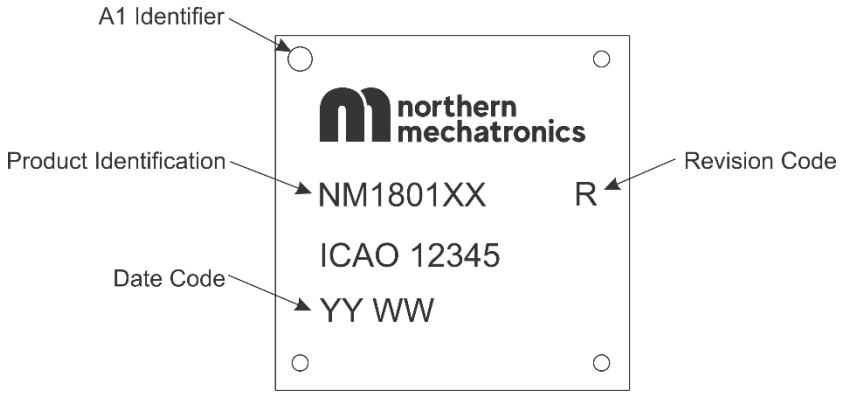

Figure 5: Device Marking

Note: Any parts marked "ES", "E", or accompanied by an Engineering Sample notification letter, are not qualified and not approved for use in production. Northern Mechatronics Inc. is not responsible for any consequences resulting from such use and will not in any event be liable for the use of engineering samples in production.

9 Packaging Specifications

9.1 Reel Specifications

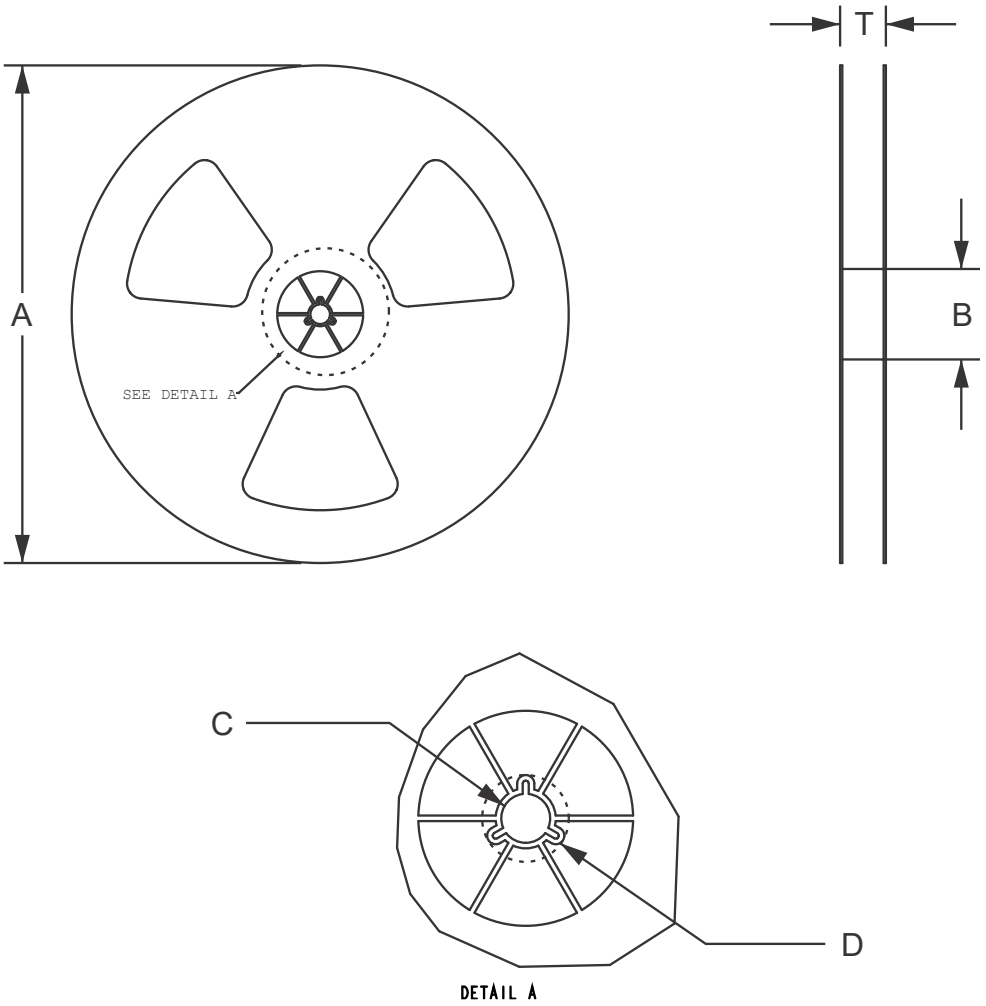

Figure 6: Reel Mechanical Specifications

Table 14: Reel Mechanical Data

Reel Diameter	Tape Size	A	B	C	D	T
330mm	24 mm	330 mm	50 mm	13 mm	20 mm	30.4 mm

9.2 Embossed Tape Specifications

The carrier tape conforms to the ANSI/EIA-481-D standard for automatic handling of surface mount components.

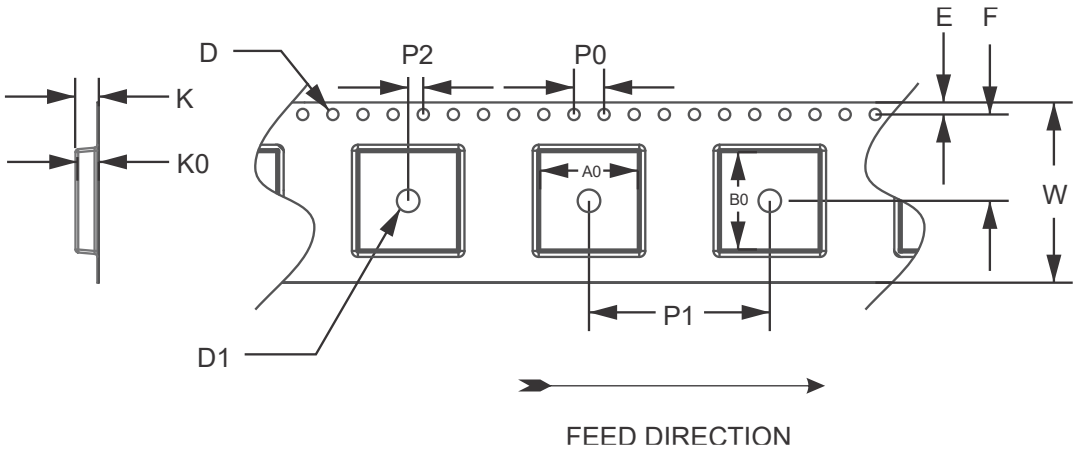

Figure 7: Tape Mechanical Specifications

Table 15: Tape Mechanical Data

Tape Size (W)	D	D1	E	F	P0	P1	P2
24 mm	1.5 mm	3 mm	1.75 mm	11.5 mm	4.0 mm	24 mm	2.0 mm

9.3 Tape Ends for Finished Goods

The trailer is a minimum of 160 mm in length, and it consists of empty cavities with sealed cover tape. The leader is a minimum of 400 mm in length, and it consists of empty cavities with sealed cover tape.

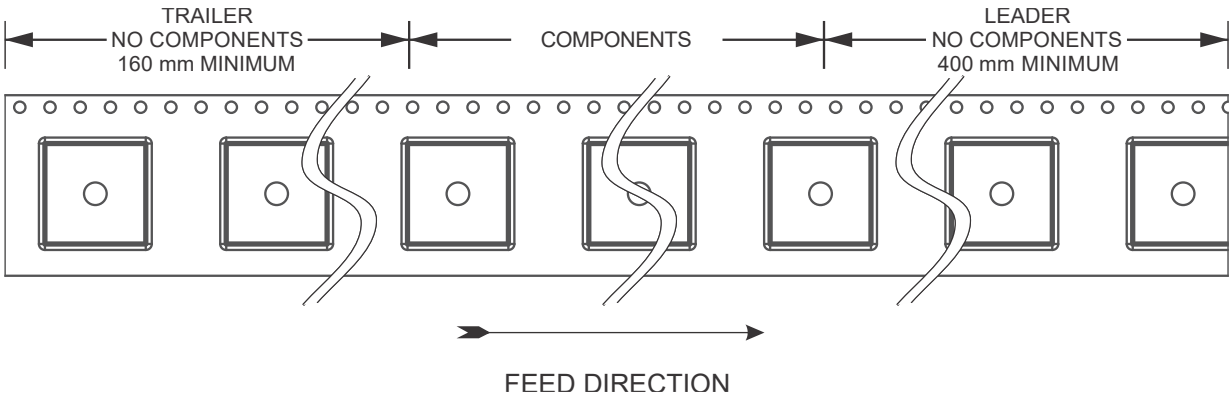

Figure 8: Tape Ends Specifications

9.4 Component Orientation

Pad A1 orientation is the upper left corner with respect to the feed direction, as shown below.

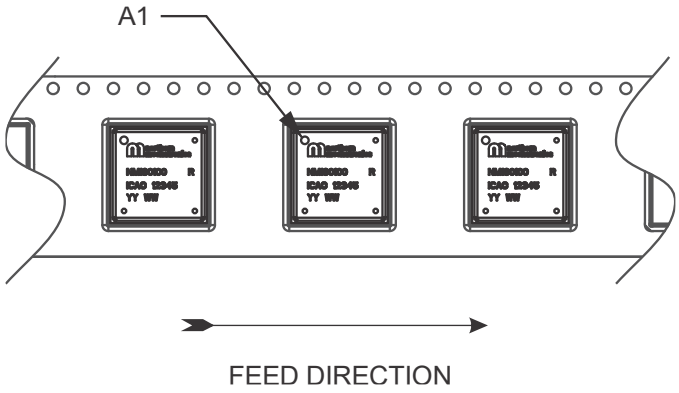

Figure 9: Component Orientation

10 Ordering Information

Model	Temperature Range	Package Description	Package Option
NM180110LTR	-40°C to +85°C	LGA 81	Tape and Reel
NM180401		NM180110 Petal Core Board	Bulk

11 References

[1] Ambiq Micro, Inc., "Apollo3 Blue Plus Datasheet," June 2024. [Online]. Available: https://ambiqmicro.com.

[2] Semtech Corporation, "SX1261-SX1262 Product Datasheet," December 2017. [Online]. Available: http://www.semtech.com.

[3] ARM Limited, "ARM Debug Interface Architecture Specification ADIv6.0," 9 March 2017. [Online]. Available: https://static.docs.arm.com/ihi0074/a/debug_interface_v6_0_architecture_specification_IHI0074A.pdf.

12 Revision History

Revision	Date	Description
A.1	October 24, 2024	Initial release.
A.2	November 19, 2024	Updated formatting standards.
A.3	December 2, 2024	Updated with minor corrections, formatting updates.